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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|----------------------------------|------------------------|
| 10/065,762 | 11/15/2002 | Wei-Pin Chen | JCLA8424 | 9203 |
| 23900 | 7590 | 06/09/2009 | | |
| J C PATENTS, INC. 4 VENTURE, SUITE 250 IRVINE, CA 92618 | | | EXAMINER NICKERSON, JEFFREY L | |
| | | | ART UNIT 2442 | PAPER NUMBER |
| | | | MAIL DATE 06/09/2009 | DELIVERY MODE PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|--------------------------------------|------------------------------------|--|
| Office Action Summary | Application No. 10/065,762 | Applicant(s) CHEN ET AL. | |
| | Examiner JEFFREY NICKERSON | Art Unit 2442 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is in response to Application No. 10/065,762 filed on 15 November 2002. The amendment presented on 18 March 2009, which provides change to claims 1-2 and 9, is hereby acknowledged. Claims 1-13 have been examined.

Claim Objections

2. The amendment presented on 18 March 2009 providing change to claims 1-2 is noted. All outstanding objections to the claims are hereby withdrawn.

Claim Rejections - 35 USC § 112

3. The amendment presented on 18 March 2009 providing change to claims 1 and 9 is noted. All outstanding rejections of the claims under 35 USC 112, second paragraph, and 35 USC 112, first paragraph, are hereby withdrawn.

Response to Arguments

4. Applicant's arguments filed on 18 March 2009 have been fully considered and are persuasive, in part, and not persuasive, in part. New rejections may appear below.

Independent claims 1 and 9

Applicant argues the combined teachings of Kawauchi (US 5,619,653), Nanba (US 4,665,484), and Fujimoto (US 5,418,913) do not teach several limitations within these

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claims. Specifically, applicant argues the combined teachings fail to render obvious the following:

“the write control unit coupled between the source controller and plurality of message rows”;

“the read control unit coupled between the destination controller and the plurality of message rows”;

Applicant's arguments are persuasive.

Applicant further argues that the proposed modification of the system would render Nanba unsatisfactory for its intended purpose. Namely, applicant argues that the distribution flag being set by the write control unit and cleared by the read control unit would not be obvious in view of Nanba, which teaches that the test-and-lock and clearing of shared resources is performed by a single processor upon accessing the shared resource.

The examiner respectfully disagrees. As indicated in the advisory action mailed 26 September 2008, Nanba's teachings provide for the following operation of the Kawauchi/Nanba/Fujimoto system: The write control unit setting the lock flag (distribution complete flag) for a message row. The write control unit writing to the message row. The write control unit clearing the lock flag. The read control unit setting the lock flag for the message row. The read control unit reading the message row. The

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read control unit clearing the lock flag. With the aforementioned use of the lock flag, the modifications to the system would not render the teachings Nanba unsatisfactory for their intended purpose, as each processor only has access to the row when they have set the lock flag. The above processing also covers the actions as claimed by applicant (setting the flag by the write control unit and clearing the flag by the read control unit). Applicant does not include language in their claim that precludes manipulation of the flag between the setting by the write control unit and the clearing by the read control unit, and, therefore, the examiner maintains the application of Nanba's teachings would not render the system unsatisfactory for its intended purpose, and the alleged limitations are taught.

Applicant's arguments are ultimately persuasive and, therefore, the rejections of these claims are hereby withdrawn.

Dependent claims 2-8 and 10-13

Applicant argues these claims conditionally on that of their parent

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

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6. Claims 1, 3, 7-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), and further in view of Giroir et al (US 4,980,852), Nanba (US 4,665,484), and Fujimoto (US 5,418,913).

Regarding claim 1, Kawauchi teaches a buffer device (Kawauchi: abstract specifies a data buffer device), for transmitting a plurality of messages between a source and destination, comprising:

a plurality of messages rows (Kawauchi: Figure 3 depicts multiple data columns), for storing the messages that the source intends to transmit to the destination (Kawauchi: abstract), each of the message rows at least comprising a write complete flag (Kawauchi: abstract specifies write attribute flags);

a write control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the source and the plurality of message rows (Kawauchi: Figure 3, see also col 4, lines 3-17), used to sequentially output a plurality of free message row addresses (Kawauchi: Figure 3; col 4, lines 3-17 specifies that the write pointer sequentially acquires buffer addresses), wherein when the message transmitting queue still has a free message row, the source controller reads an address of a target message row that is currently free among said plurality of message rows (Kawauchi: Figure 3; col 4, lines 3-17; col 4, lines 45-58 specifies it does not use addresses if they've already been written to), and when the source completes writing a message of the target message row, the write complete flag of the target message row is set by the write control unit

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(Kawauchi: Figure 3, col 4, lines 3-17; col 4, lines 45-58 specifies the write attribute bit is flagged once writing is complete), and when the message transmitting queue has no free message row, said write control unit outputs a non-free message row signal (Kawauchi: Figure 3, item 100; col 3, lines 31-57 specify there is a “reception ready” signal for the buffer device, equivalent to a NOT “not free address” signal and used for the same purpose);

and a read control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the destination and the plurality of message rows (Kawauchi: Figure 3; see also col 3, lines 23-57), to read the message of the target message row when the write complete flag of the target message row is set, wherein once the destination completes reading the message of the target message row, the write complete flag of the target message row is cleared is cleared by the read control unit (Kawauchi: col 5, lines 22-35).;

wherein the shared resource is a plurality of message rows (Kawauchi: Fig. 2).

Kawauchi does not teach the use of a distribution complete flag, wherein the distribution complete flag is set by the write control unit when the shared resource has began to be used, and wherein the distribution complete flag is cleared by the read control unit after the use of the shared resource;

issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request;

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wherein the write control unit is coupled between the source controller and the shared resource;

wherein the read control unit is coupled between the destination controller and the shared resource; or

wherein the shared resource are coupled between the write control unit and the read control unit.

Giroir, in a similar field of endeavor, teaches wherein the write control unit is coupled between the source controller and the shared resource (Giroir: Figure 6, item 610; Figure 7A; col 4, lines 43 – col 6, line 18 provides each unit has their own control unit between them and the shared resource);

wherein the read control unit is coupled between the destination controller and the shared resource (Giroir: Figure 6, item 620; Figure 7B; col 4, line 43 – col 6, line 18 provides each unit has their own control unit between them and the shared resource);

wherein the shared resource are coupled between the write control unit and the read control unit (Giroir: Figure 1; Figure 6, item 640; col 4, line 43 – col 5, line 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Giroir for having separate control units for both the source and destination. The teachings of Giroir, when implemented in the Kawauchi system, will allow one of ordinary skill in the art to have a send/receive control unit for each controller that manages interactions with the message queue. One of

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ordinary skill in the art would be motivated to utilize the teachings of Giroir in the Kawauchi system in order to manage the interface between the controllers and shared message rows.

The Kawauchi/Giroir system does not teach the use of a distribution complete flag, wherein the distribution complete flag is set by the write control unit when the shared resource has began to be used, and wherein the distribution complete flag is cleared by the read control unit after the use of the shared resource; or

issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request.

Nanba, in a similar field of endeavor, the use of a distribution complete flag, wherein the distribution complete flag is set by the write control unit when the shared resource has began to be used, and wherein the distribution complete flag is cleared by the read control unit after the use of the shared resource (Nanba: col 1, lines 17 – col 2, line 41 specifies a test and set instruction, which uses a lock control flag on shared memory).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Nanba for using a test and set instruction. The teachings of Nanba, when implemented in the Kawauchi/Giroir system, will allow one of ordinary skill in the art to handle multithreaded accesses to shared memory. One of ordinary skill in the art would be motivated to utilize the teachings of Nanba in

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the Kawauchi/Giroir system in order to prevent race conditions during accessing of shared memory by multiple threads.

The Kawauchi/Giroir/Nanba system does not teach issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request.

Fujimoto, in a similar field of endeavor, teaches issuing a read request for informing the destination to read the shared data and subsequently reading the data in response to the read request (Fujimoto: Figure 4, "Receiver's Identity" rows; Figure 6, item 110; col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Fujimoto for sending interrupts to receiving processors identifying that data is ready to be read. The teachings of Fujimoto, when implemented in the Kawauchi/Giroir/Nanba system, will allow one of ordinary skill in the art to utilize organized reading from destination controllers by using interrupts. One of ordinary skill in the art would be motivated to utilize the teachings of Fujimoto in the Kawauchi/Giroir/Nanba system in order to allow efficient and quick reading of a queue from multiple processors by using interrupts.

Regarding claim 3, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein the read control unit comprises:

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a read pointer control unit, to store a read address of the message transmitting queue (Kawauchi: Figure 3, item 103), wherein when the destination controller completes reading the message of the message row pointed to by the read address, said read pointer control unit clears the distribution complete flag and the write complete flag of the message row pointed to by the read address (Kawauchi: Figure 3, items 102 and 103; col 5, lines 22-35; Nanba: col 1, lines 17-45), and progresses the read address (Kawauchi: abstract specifies reading is sequential);

a read buffer, coupled to the read pointer control unit and the plurality of message rows, to temporarily store the message of the message row pointed to by the read address (Fujimoto: Figure 10, items 115 provides the receiving processor is storing the message);

and a read request multiplexer, coupled to the read pointer control unit and the write complete flags of the plurality of message rows, to output the read request according to the write complete flag of the message row pointed to by the read address (Fujimoto: col 1, line 50 – col 2, line 6 specifies that obtaining read pointer address from flag status in a queue is well known in the art).

Regarding claim 7, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein the source is a central processing unit (Fujimoto: Figure 1a, item 1 and Figure 9, items 114).

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Regarding claim 8, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein the destination is a central processing unit (Fujimoto: Figure 1a, item 2 and Figure 9, items 114).

Regarding claim 9, this method claim comprises limitations corresponding to that of claim 1 and the same rationale of rejection is used, where applicable; and

wherein the rows are referenced with read and write pointers (Kawauchi: Figure 3, item 102; Figure 3, item 103) with the write control unit and read control unit (Giroir: abstract; col 2, lines 20-31).

Regarding claim 10, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein when the write pointer is progressed and points to a message row whose distribution complete flag is set, a not free message row signal is asserted to inform the source controller.

Regarding claim 11, this method claim comprises limitations corresponding to that of claim 7 and the same rationale of rejection is used, where applicable.

Regarding claim 12, this method claim comprises limitations corresponding to that of claim 8 and the same rationale of rejection is used, where applicable.

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Regarding claim 13, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein the read request is an interrupt request of the CPU (Fujimoto: col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

7. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Giroir et al (US 4,980,852), Nanba (US 4,665,484), and Fujimoto (US 5,418,913), and in further view of Fried et al (US 5,142,676).

Regarding claim 2, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein the write control unit comprises:

a write pointer control unit (Kawauchi: Figure 3, item 102), for storing a write address of the target message row (Kawauchi: col 4, lines 3-17), wherein after the source controller reads the write address of the target message row, said write pointer control unit sets the distribution complete flag of the target message row (Nanba: col 1, lines 17-45 specifies a test and set instruction, which uses a lock control flag on shared memory), and progresses the write address of the target message row (Kawauchi: col 4, lines 3-17 provide the write addresses are progressed sequentially), and when the source controller completes writing the message of the target message row, the write pointer control unit sets the write complete flag of the target message row (Kawauchi: col 4, lines 46-58 specifies changing the write data attribute flag after writing data);

The Kawauchi/Giroir/Nanba/Fujimoto system does not teach further comprising:

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a distribution complete flag multiplexer, coupled to the write pointer control unit and the distribution complete flags of the plurality of message rows, to output a non-distributed signal according to the distribution complete flag of the message row pointed to by the write address; or

a distribution address multiplexer, coupled to the distribution complete flag multiplexer and the write pointer control unit, to alternatively output one of the write address and the no free message row signal according to the not-distributed signal.

Fried, in a similar field of endeavor, teaches:

a distribution complete flag multiplexer (Fried: Figure 2, item 62), coupled to the write pointer control unit (Fried: Figure 3, item 85; col 6, lines 24-39) and the distribution complete flags of the plurality of message rows, (Fried: Figure 2, items 58; col 5, lines 28-33) to output a not-distributed signal (Fried: NOT FOUND signal) according to the distribution complete flag of the message row pointed to by the write address (Fried: col 7, lines 37-63 specifies that if a shared memory row has been already locked, a NOT FOUND signal is used to indicate the row can't be accessed);

and a distribution address multiplexer (Fried: Figure 3, items 102, 104, 106; col 7, lines 20-36), coupled to the distribution complete flag multiplexer and the write pointer control unit, to alternatively output one of the write address and the no free message row signal according to the not-distributed signal (Fried: col 7, lines 20-63 specify that when it is determined the segment address has not been locked, then the LOCK signal is applied to lock the segment and then the segment is written to; and when it is

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determined the segment address has been locked the DISALLOW signal is asserted;
See also col 6, lines 24-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Fried for managing locked memory segments with NOT FOUND and DISALLOW signals. The teachings of Fried, when implemented in the Kawauchi/Giroir/Nanba/Fujimoto system, will allow one of ordinary skill in the art to identify memory segments of the queue between two processors that have been locked and disallow writing to locked segments while allowing locking and writing to unlocked segments. One of ordinary skill in the art would be motivated to utilize the teachings of Fried in the Kawauchi/Giroir/Nanba/Fujimoto system in order to allow multiple processors to identify which memory segments are currently locked and which are available for locking and writing.

Regarding claim 10, this claim contains limitations found within and corresponding to claim 2 and the same rationale of rejection is applied, where applicable.

8. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Giroir et al (US 4,980,852), Nanba (US 4,665,484), and Fujimoto (US 5,418,913), and in further view of Balmer et al (US 5,724,599).

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Regarding claim 4, the Kawauchi/Giroir/Nanba/Fujimoto system teaches wherein each message row comprises data the source intends to transmit to the destination

(Kawauchi: abstract).

The Kawauchi/Giroir/Nanba/Fujimoto system does not teach wherein the data is a command row, to store a command, and a data row, to store data.

Balmer, in a similar field of endeavor, teaches wherein the data is a command (instruction) row, to store a command, and a data row (Balmer: Figure 2, items 11, 12, 13, 14), to store data.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Balmer for splitting data into instruction rows and data rows. The teachings of Balmer, when implemented in the Kawauchi/Giroir/Nanba/Fujimoto system, will allow one of ordinary skill in the art to organize data sending from one processor to the next by splitting it into instructions and data. One of ordinary skill in the art would be motivated to utilize the teachings of Balmer in the Kawauchi/Giroir/Nanba/Fujimoto system in order to allow the receiving processor to easily identify which part of the message is an instruction and which part is data.

Regarding claim 5, the Kawauchi/Giroir/Nanba/Fujimoto/Balmer system teaches wherein the size of the command row is four bytes (Balmer: col 10, line 52 – col 11, line 10 specify 32 bit instructions).

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Regarding claim 6, the Kawauchi/Giroir/Nanba/Fujimoto/Balmer system teaches wherein the size of the data row is a multiple of four bytes (Balmer: col 10, line 52 – col 11, line 10 specify data is stored in 32 bit words).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY NICKERSON whose telephone number is (571)270-3631. The examiner can normally be reached on M-Th, 9:00am - 7:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571)272-3868. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. N./
Jeffrey Nickerson
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